IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 08/842,230
Priority Filing Date ..... April 22, 1997
Inventor ..... Luan Tran et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2814
Priority Examiner ..... H. Weiss
Attorney's Docket No. MI22-1784
Title: Memory Integrated Circuitry

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: Frederick M. Fliegel, Ph.D.
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Sir:

This is a preliminary amendment accompanying a Request for Continuation Application for the above-entitled patent application. Prior to examining the application, please enter the following amendments.

AMENDMENTS

In the Specification

At page 1, before the **TECHNICAL FIELD** insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Continuation Application of U.S. Patent Application Serial No. 08/842,230, filed on April 22, 1997, entitled "Memory

Integrated Circuitry" and naming Luan Tran and Alan R. Reinberg as inventors, the disclosure of which is hereby incorporated herein by reference.

Replace the paragraph beginning on page 9, line 22, and extending through p. 9, line 23, with:

U.S. patent application serial number 08/530,661 listing Brent Keeth and Pierre Fazan as inventors discloses methods which can be utilized for forming the structures disclosed herein (such as, for example, dry oxidation for formation of LOCOS), and is hereby incorporated by reference.

At p. 11, line 2, after CLAIMS, insert We claim:

In the Drawings

Fig. 2 has been amended as shown in the marked-up-in-red drawing enclosed herewith. Revised formal drawing is also included.

In the Claims

1. Memory integrated circuitry comprising:

an array of memory cells formed in lines over a semiconductive substrate and occupying area thereover, the respective area consumed by at least some individual memory cells within the array being equal to less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by LOCOS field oxide formed therebetween.

2. The memory integrated circuitry of claim 1 wherein the memory cells comprise DRAM cells.

3. (Amended) The memory integrated circuitry of claim 1 wherein individual ones of the lines of memory cells are substantially straight throughout the array.

4. The memory integrated circuitry of claim 1 wherein the LOCOS field oxide between adjacent lines is less than or equal to 2500 Angstroms thick.

5. The memory integrated circuitry of claim 1 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $7F^2$.

6. The memory integrated circuitry of claim 1 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $6F^2$.

7. (Amended) Memory integrated circuitry comprising:

an array of memory cells formed over a semiconductive substrate and occupying area thereover, at least some memory cells of the array being formed in lines of active area formed within the semiconductive substrate which are continuous between adjacent memory cells, said adjacent memory cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent memory cells;

the respective area consumed by individual ones of said adjacent memory cells being equal to less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by LOCOS field oxide formed therebetween.

8. (Amended) The memory integrated circuitry of claim 7 wherein individual ones of the lines of continuous active area are substantially straight throughout the array.

9. The memory integrated circuitry of claim 7 wherein the LOCOS field oxide between adjacent lines is less than or equal to 2500 Angstroms thick.

10. The memory integrated circuitry of claim 7 wherein the memory cells comprise DRAM cells.

11. The memory integrated circuitry of claim 7 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $7F^2$.

12. The memory integrated circuitry of claim 7 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $6F^2$.

13. (Amended) Dynamic random access memory circuitry comprising:

an array of word lines and bit lines formed over a semiconductive substrate defining an array of DRAM cells occupying area over the semiconductive substrate, at least some DRAM cells of the array being formed in lines of active area formed within the semiconductive substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent DRAM cells;

the respective area consumed by individual ones of said adjacent memory cells being equal to less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by LOCOS field oxide formed therebetween; and

the bit lines comprise D and D^* lines formed in a folded bit line architecture within the array.

14. (Amended) The memory integrated circuitry of claim 13 wherein individual ones of the lines of continuous active area are substantially straight throughout the array.

15. The memory integrated circuitry of claim 13 wherein the LOCOS field oxide between adjacent lines is less than or equal to 2500 Angstroms thick.

16. The memory integrated circuitry of claim 13 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $7F^2$.

17. The memory integrated circuitry of claim 13 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $6F^2$.

18. (Amended) Dynamic random access memory circuitry comprising:

an array of word lines and bit lines formed over a bulk silicon semiconductive substrate defining an array of DRAM cells occupying area over the semiconductive substrate, the word lines and bit lines having respective conductive widths which are less than or equal to 0.25 micron, the DRAM cells within the array being formed in lines of active area formed within the silicon substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by respective conductive lines formed over said continuous active area between said adjacent DRAM cells;

at least some adjacent lines of continuous active area within the array being isolated from one another by LOCOS field oxide formed therebetween, said LOCOS field oxide having a thickness of no greater than 2500 Angstroms;

the respective area consumed by individual ones of said adjacent memory cells being equal to less than 0.5 micron^2; and

the bit lines comprise D and D* lines formed in a folded bit line architecture within the array.

19. (Amended) The memory integrated circuitry of claim 18 wherein individual ones of the lines of continuous active area are substantially straight throughout the array.

20. The memory integrated circuitry of claim 18 wherein said respective area consumed by at least some individual memory cells within the array is no greater than 0.4375 $micron^2$.

21. The memory integrated circuitry of claim 18 wherein said respective area consumed by at least some individual memory cells within the array is no greater than 0.375 $micron^2$.

22. (Amended) Dynamic random access memory circuitry comprising:

an array of word lines and bit lines formed over a semiconductive substrate defining an array of DRAM cells occupying area over the semiconductive substrate, at least some DRAM cells of the array being formed in lines of active area formed within the semiconductive substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent DRAM cells;

the respective area consumed by individual ones of said adjacent memory cells being equal to less than $8F^2$, where "F" is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

the bit lines comprise D and D^* lines formed in a folded bit line architecture within the array.

23. (Amended) The memory integrated circuitry of claim 22 wherein individual ones of the lines of continuous active area are substantially straight throughout the array.

24. The memory integrated circuitry of claim 22 wherein F is no greater than 0.25 micron.

25. The memory integrated circuitry of claim 22 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $7F^2$.

26. The memory integrated circuitry of claim 22 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $6F^2$.

New Claims

27. A method of forming integrated circuitry, comprising:

forming LOCOS field oxide by providing nitride masking blocks over a silicon substrate; the nitride masking blocks being separated by spaces that are less than or equal to 0.25 micron; the spaces leaving portions of the underlying semiconductor substrate exposed between the nitride masking blocks; subjecting the substrate to dry oxidation to form isolation oxide within the spaces and then removing the nitride masking blocks; and

forming an array of memory cells in lines over the semiconductive substrate and occupying area thereover, the respective area consumed by at least some individual memory cells within the array being less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; at least some of the minimum pitch

adjacent lines of memory cells within the array being isolated from one another by the LOCOS field oxide.

28. The method of claim 27 wherein the lines of memory cells are substantially straight throughout the array.

29. The method of claim 27 wherein the LOCOS field oxide between adjacent lines is formed to be less than or equal to 2500 Angstroms thick.

30. The method of claim 27 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $7F^2$.

31. The method of claim 27 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $6F^2$.

32. A method of forming memory integrated circuitry, comprising:

forming LOCOS field oxide by providing nitride masking blocks over a silicon substrate; the nitride masking blocks being separated by spaces that are less than or equal to 0.25 micron; the spaces leaving portions of the underlying semiconductor substrate exposed between the nitride masking blocks; subjecting the substrate to dry oxidation to form isolation oxide within the spaces and then removing the nitride masking blocks; and

forming an array of memory cells over the semiconductive substrate and occupying area thereover, at least some memory cells of the array being formed in lines of active area formed within the semiconductive substrate which are continuous between adjacent memory cells, said adjacent memory cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent memory cells; the respective area consumed by individual ones of said adjacent memory cells being less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by the LOCOS field oxide.

33. A method of forming dynamic random access memory circuitry, comprising:

forming LOCOS field oxide by providing nitride masking blocks over a silicon substrate; the nitride masking blocks being separated by spaces that are less than or equal to 0.25 micron; the spaces leaving portions of the underlying semiconductor substrate exposed between the nitride masking blocks; subjecting the substrate to dry oxidation to form isolation oxide within the spaces and then removing the nitride masking blocks;

forming an array of word lines and bit lines over the semiconductive substrate to define an array of DRAM cells occupying area over the semiconductive substrate, at least some DRAM cells of the array being formed in lines of active area formed within the semiconductive substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent DRAM cells; the respective area consumed by individual ones of said adjacent memory cells being less than $8F^2$, where "F" is greater than 0 micron and no greater than 0.25 micron and is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; at least some of the minimum pitch adjacent lines of memory cells

within the array being isolated from one another by the LOCOS field oxide; and

wherein the bit lines are formed to comprise D and D* lines arranged in a folded bit line architecture within the array.

34. A method of forming dynamic random access memory circuitry, comprising:

forming LOCOS field oxide by providing nitride masking blocks over a semiconductor substrate; the nitride masking blocks being separated by spaces that are less than or equal to 0.25 micron; the spaces leaving portions of the underlying semiconductor substrate exposed between the nitride masking blocks; subjecting the substrate to dry oxidation to form isolation oxide within the spaces and then removing the nitride masking blocks;

forming an array of word lines and bit lines over the bulk silicon semiconductive substrate to define an array of DRAM cells occupying area over the semiconductive substrate, the word lines and bit lines having respective conductive widths which are greater than 0 micron and less than or equal to 0.25 micron, the DRAM cells within the array being formed in lines of active area formed within the silicon substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by respective conductive lines formed over said continuous active area between said adjacent DRAM cells; at least some adjacent lines of continuous active area within the array being isolated from one another by the LOCOS field oxide, said LOCOS field oxide having a thickness of no greater than 2500 Angstroms; the respective area consumed by individual ones of said adjacent memory cells being less than 0.5 micron^2; and

wherein the bit lines are formed to comprise D and D* lines arranged in a folded bit line architecture within the array.

35. The method of claim 27, wherein forming an array of memory cells in lines comprises forming an array of memory cells coupled to an array of word lines and bit lines, wherein the bit lines are formed to comprise D and D* lines arranged in a folded bit line architecture within the array.

36. The method of claim 27, wherein forming an array of memory cells in lines comprises forming an array of memory cells coupled to an array of word lines and bit lines, wherein the bit lines are orthogonal to the word lines.

37. The method of claim 32, wherein forming an array of memory cells comprises forming an array of memory cells coupled to an array of word lines and bit lines, wherein the bit lines are formed to comprise D and D* lines arranged in a folded bit line architecture within the array.

38. The method of claim 32, wherein forming an array of memory cells comprises forming an array of memory cells coupled to an array of word lines and bit lines, wherein the bit lines are orthogonal to the word lines.

39. The method of claim 32, wherein forming an array of word lines and bit lines comprises forming the bit lines and the word lines to be orthogonal.

40. The method of claim 32, wherein forming an array of word lines and bit lines comprises forming the bit lines in a folded bit line architecture within the array.

41. A method of forming dynamic random access memory circuitry, comprising:

forming LOCOS field oxide by providing nitride masking blocks over a silicon substrate; the nitride masking blocks being separated by spaces that are less than or equal to 0.25 micron; the spaces leaving portions of the underlying semiconductor substrate exposed between the nitride masking blocks; subjecting the substrate to oxidation to form isolation oxide within the spaces and then removing the nitride masking blocks; and

forming an array of word lines and bit lines over the semiconductive substrate to define an array of DRAM cells occupying area over the semiconductive substrate, at least some DRAM cells of the array being formed in lines of active area formed within the semiconductive substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent DRAM cells; the respective area consumed by individual ones of said adjacent memory cells being less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by the LOCOS field oxide.

42. The method of claim 41, wherein forming an array of word lines and bit lines comprises forming the bit lines and the word lines to be orthogonal.

43. The method of claim 41, wherein the bit lines are formed to comprise D and D* lines arranged in a folded bit line architecture within the array.

REMARKS

Claims 3, 7, 8, 13, 14, 18, 19, 22 and 23 have been amended and new claims 27-43 have been added. Claims 1-43 are pending in the application.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

The amendments to the claims address minor informalities noted during review, and do not alter the scope of the claims. No new matter is added by the amendments to the claims.

The amendments to the specification provide priority information and correct minor informalities noted during review. No new matter is added by the amendments to the specification.

Fig. 2 has been amended as shown in the marked-up-in-red drawing enclosed herewith to correct minor informalities noted during review. No new matter has been added by the amendment to the drawings. The Examiner's approval of the amendments to the drawing is respectfully requested.

New claims 27-43 are similar to claims that have been allowed in the parent case, but differ in scope. New claims 27-43 are supported at least by text appearing at p. 6, line 17 through p. 9, line 23 of the specification as originally filed. No new matter is added by new claims 27-43.

This application is believed to be in condition for allowance and action to that end is requested. The Examiner is requested to telephone the undersigned in the event that the next office action is one other than a Notice

of Allowance. The undersigned is available during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: Aug. 14, 2001

By: ______________________

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